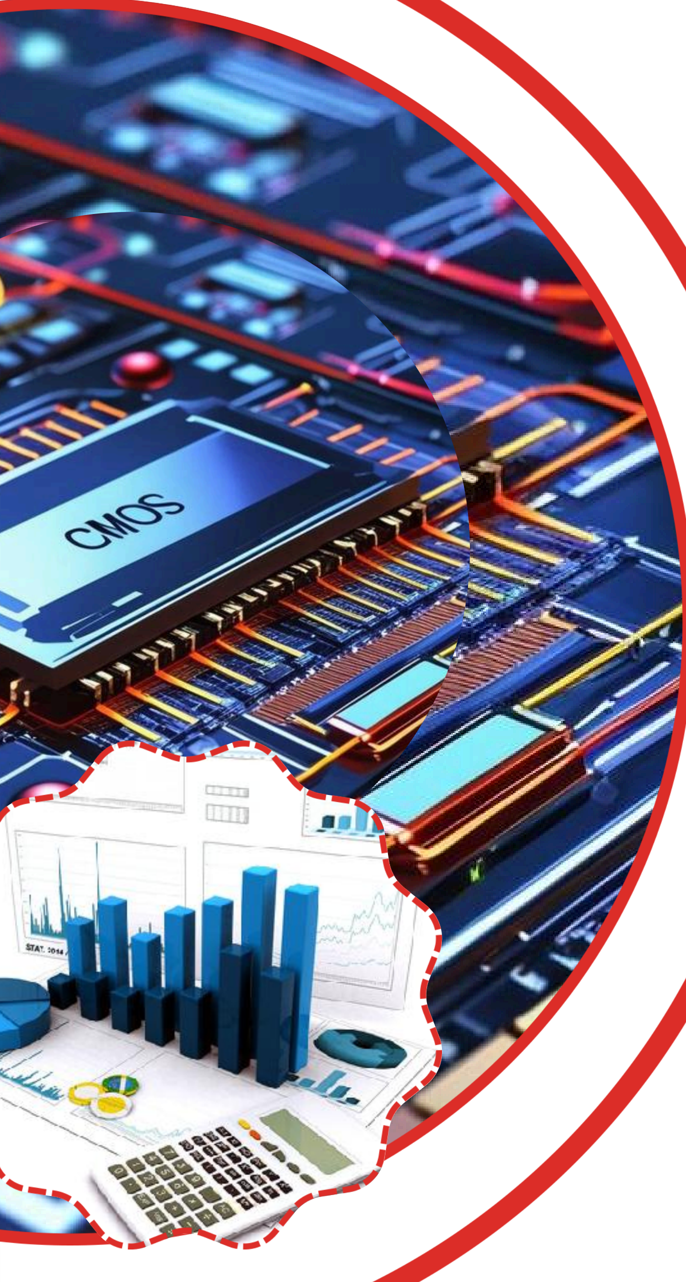
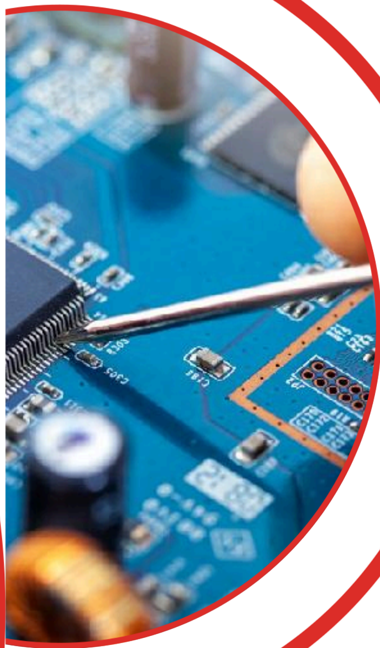
KEMENTERIAN PENDIDIKAN TINGGI
JABATAN PENDIDIKAN POLITEKNIK DAN KOLEJ KOMUNITI

POLITEKNIK MALAYSIA MERLIMAU

INTEGRATED CIRCUIT FABRICATION PROCESS

IC TESTING RELIABILITY FAILURE ANALYSIS





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Hakcipta terpelihara. Tiada bahagian terbitan ini boleh diterbitkan semula atau ditukar dalam apa jua bentuk dengan cara apa jua sama ada secara elektronik, mekanikal, fotokopi, rakaman dan sebagainya sebelum mendapat kebenaran bertulis daripada Pengarah Politeknik Merlimau Melaka.

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Preface

Integrated circuits (ICs) are at the core of today's technology — powering smartphones, computers, and industrial systems. Understanding how ICs are tested, evaluated, and maintained for reliability is a key foundation for future engineers and technologists.

This eBook, "IC Testing, Reliability and Failure Analysis," is part of the **Integrated Circuit Fabrication Process** learning series. It introduces students to essential post-fabrication concepts including IC testing, reliability prediction, degradation behavior, and failure analysis.

To enhance understanding, this eBook integrates interactive learning elements such as videos for visual demonstration, quizzes for self-assessment, and illustrations to support conceptual clarity. These features aim to make learning more engaging, dynamic, and aligned with real-world semiconductor practices.

Each chapter progresses from fundamental theory to practical applications, allowing students to connect knowledge with real industry situations.

We hope this eBook encourages curiosity, strengthens understanding, and inspires students to explore deeper into the fascinating world of microelectronics.

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Politeknik Merlimau Melaka
2025

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INTRODUCTION

Integrated Circuits (ICs) are the foundation of modern electronics, powering devices from smartphones to industrial systems. To ensure these tiny components function reliably, every IC must undergo a series of testing and evaluation processes after fabrication.

This eBook explores three key aspects of post-fabrication study:

1. **IC Testing** – verifying circuit performance at wafer and final product stages.
2. **Reliability** – predicting and improving IC lifespan and stability.
3. **Failure Analysis** – identifying and understanding defects to enhance manufacturing quality.

Through clear explanations and interactive elements, this eBook helps students understand the importance of testing, reliability, and analysis in producing high-performance microelectronic devices — building a strong foundation for future study and careers in semiconductor technology.

IC TESTING

IC testing, reliability, and failure analysis are critical components in the design and fabrication of CMOS (Complementary Metal-Oxide-Semiconductor) integrated circuits.

2.1 Electrical Evaluation of IC (Wafer Testing)

Before integrated circuits (ICs) are separated into individual chips and packaged, they go through a process called electrical evaluation while still in wafer form. This step is essential to make sure the ICs are functioning properly before moving on to final assembly.

The two main types of testing at this stage are **Test Pattern Testing** and **Probe Testing**.

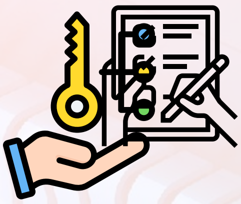
A. Test Pattern Testing

What is?

Test pattern testing is a method where predefined sets of digital signals (known as test vectors) are applied to the IC's input pins. The response from the IC is then observed and compared to the expected output.

PURPOSE

This testing checks the logical correctness and performance of the IC’s internal circuitry. It helps to verify whether the design has been implemented correctly and whether the chip responds as intended in a simulated real-world situation.



- Ensures the logic gates and functional blocks inside the chip are working.
- Can identify design errors, process variations, or faults like short circuits or open connections.
- Often performed using automated test equipment (ATE).

B. Probe Testing

What is?

Probe testing (also called wafer probing) involves physically contacting tiny metal pads on the surface of each die (individual chip on the wafer) using microscopic needles called **probe needles**.

PURPOSE

This step checks the electrical characteristics (like voltage, current, resistance) of the chip while it is still on the wafer. It helps detect defective dies early in the process, so that only working chips proceed to packaging.

See HOW IT Works

- A machine called a probe station aligns and lowers fine needles onto the pads of each die.
- Electrical signals are sent through the needles, and the chip's response is measured.
- Dies that fail are marked or recorded so they can be discarded later.

2.2 Final Product Testing

After the individual dies (chips) are packaged into their final form (such as DIP, QFP, or BGA packages), they undergo a final round of testing called **Final Testing** or **Product Testing**. This is the last chance to catch any faults before the ICs are shipped to customers or integrated into electronic products.

2.2 Burn It Testing

Burn-in is the process of stressing semiconductor to weed out potentially weak circuits. The technique involved subjecting a device to high temperature and voltage stress for several hours or days and exercising it through the limits of its electrical performance. This is the only effective method of assuring high reliability of semiconductor is to perform Burn-in.

What is?

Burn-In Testing is a special type of stress test where ICs are exposed to extreme operating conditions — typically **high temperature** and **higher-than-normal voltage** — for an extended period of time.

PURPOSE

To accelerate potential early-life failures. It also known as **infant mortality**.

Weak or marginal chips will fail during burn-in, allowing only strong ICs to move forward.

See How It Works

- ICs are placed into a burn-in oven or chamber.
- The environment simulates stressful real-world conditions.
- The chips are run continuously for several hours or days.
- Failures are logged, and failed chips are removed.

Summary

Testing Type	Description	Purpose
Test Pattern Testing	Sends signal patterns to simulate operations	Checks logic correctness
Probe Testing	Uses needles to contact wafer chip pads	Measures electrical performance per die

Test Type	Description	Purpose
Final Testing	Tests packaged ICs for function, performance, specs	Ensures only working chips are shipped
Burn-In Testing	Stress test under high temp/voltage	Eliminates weak ICs and increases reliability

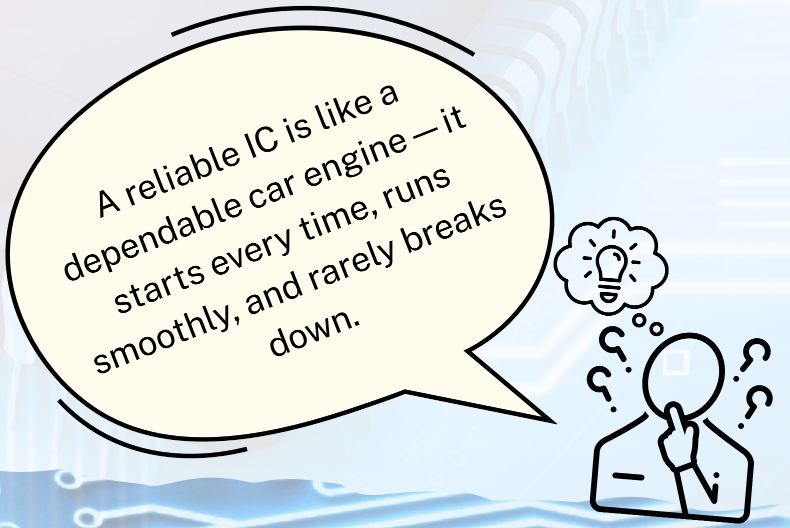
RELIABILITY

Reliability is the ability of a technique to produce quality consistently. Reliability of semiconductor devices may depend on assembly, use, and environmental conditions. Stress factors affecting device reliability include gas, dust, contamination, voltage, current density, temperature, humidity, mechanical stress, vibration, shock, radiation, pressure and intensity of magnetic and electrical fields. Design factor affecting semiconductor reliability include voltage derating, power derating, current derating, metastability, logic timing margins, timing analysis, temperature derating, and process control.

3.1 Meaning of Reliability

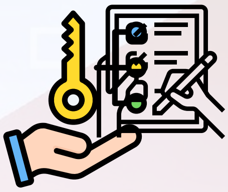
What is?

Reliability refers to the ability of an integrated circuit to perform its intended function consistently and correctly over a specified period, under specified environmental and operating conditions.



PURPOSE

The main purpose of ensuring reliability in integrated circuits (ICs) is to guarantee that electronic devices perform correctly and consistently over time.



- **Consistency**: The IC should operate the same way every time.
- **Durability**: It should last for the expected product lifespan.
- **Stability**: Should function correctly under normal and even slightly stressful conditions (like heat or voltage fluctuation).

Reliability is a critical concern in integrated circuits, especially in applications where failure could lead to significant damage, danger, or financial loss.

Imagine a phone that crashes every time it gets slightly hot — annoying, right?

3.2

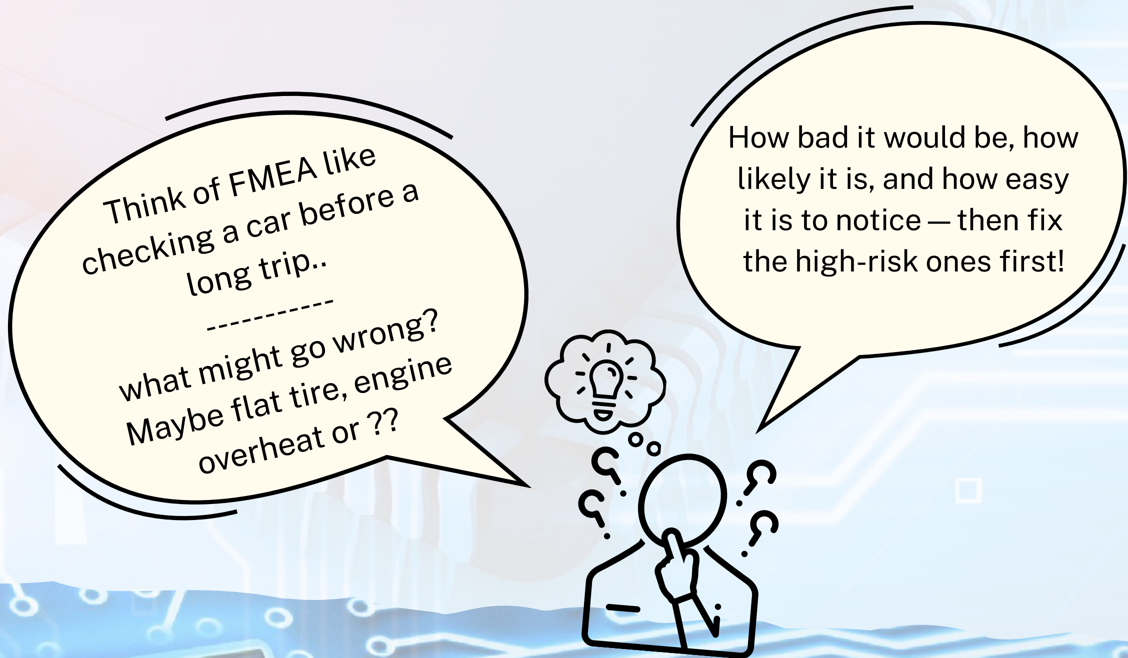
Reliability Prediction Technique

Customers are placing increased demands on companies for high quality, reliable products. The increasing capabilities and functionality of many products are making it more difficult for manufacturers to maintain the quality and reliability.

Traditionally, reliability has been achieved through extensive testing and use of techniques such as probabilistic reliability modelling.

There are techniques done in the late stages of development. The challenge is to design in quality and reliability early in development cycle.

In the development of integrated circuits (ICs), predicting how and why a failure might happen is crucial to improving reliability. One widely used technique for this is called **FMEA**, which stands for **Failure Mode and Effects Analysis.**



3.3

Failure Mode and Effects Analysis (FMEA)

What is?

FMEA is a structured and systematic approach used by engineers to identify:

- Possible failure modes (How a component might fail),
- Their causes and effects on the system, and
- How critical each failure is to the overall product reliability.

PURPOSE

- To predict potential reliability issues before they occur.
- To help designers and manufacturers prioritize risks and take action early.
- To reduce failure rates during production and in the field.

The early and consistent use of FMEA in the design process allows the engineer to design out failures and produce reliable, safe and customer pleasing products. FMEA also capture historical information for use in product improvement.

The early and consistent use of FMEA in the design process allows the engineer to design out failures and produce reliable, safe and customer pleasing products. FMEA also capture historical information for use in product improvement.

TYPES

1. **Design FMEA (DFMEA)**:
   → Focuses on failure risks in the IC design stage (e.g., logic errors, layout flaws).
2. **Process FMEA (PFMEA)**:
   → Focuses on potential failures during manufacturing and testing (e.g., contamination, incorrect etching, bonding issues).

Benefit using FMEA

- ✅ Detects design and process weaknesses early
- ✅ Improves overall product reliability
- ✅ Saves cost by reducing late-stage redesign or field failures
- ✅ Enhances customer satisfaction and safety

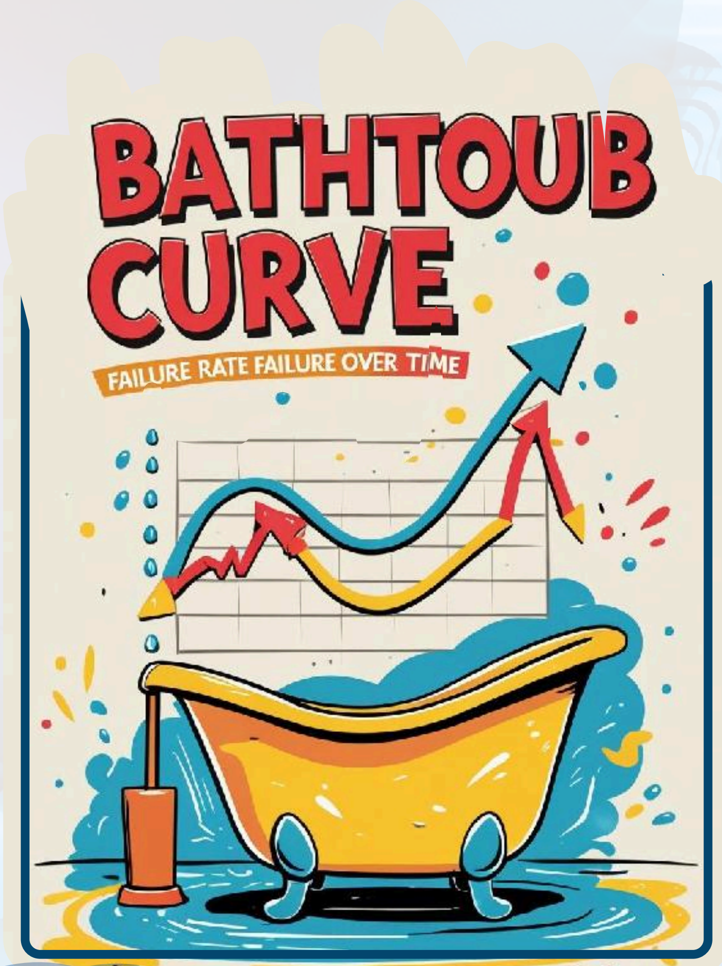
3.4 Bathtub Curve Prediction of Reliability

The bathtub curve is a common way to describe how the failure rate of an integrated circuit (IC) changes over its lifetime. The shape of the graph looks like a bathtub — high at the beginning and end, and low in the middle.

It is divided into **three main phases:**

a. Infant mortality
b. Operating life
c. Wear out

The bathtub curve is generated by mapping the rate of early "infant mortality" failures when first introduced, the rate of random failures with constant failure rate during its "useful life", and finally the rate of "wear out" failures as the product exceeds its design lifetime.



A. Infant mortality

What is?

This is the early-life stage of the IC, right after it is manufactured and starts being used. The failure rate is high at first because some defects from the fabrication process (like dust contamination, microscopic cracks, or bonding issues) may not have been caught during testing.

CAUSES FAILURE

- Manufacturing defects
- Material flaws
- Poor assembly or packaging
- Weak connections

REDUCE

Use burn-in testing to stress the IC and filter out weak units before shipping.

Like new shoes — some may have hidden flaws that only show up after the first few wears.

B. Operating life

What is?

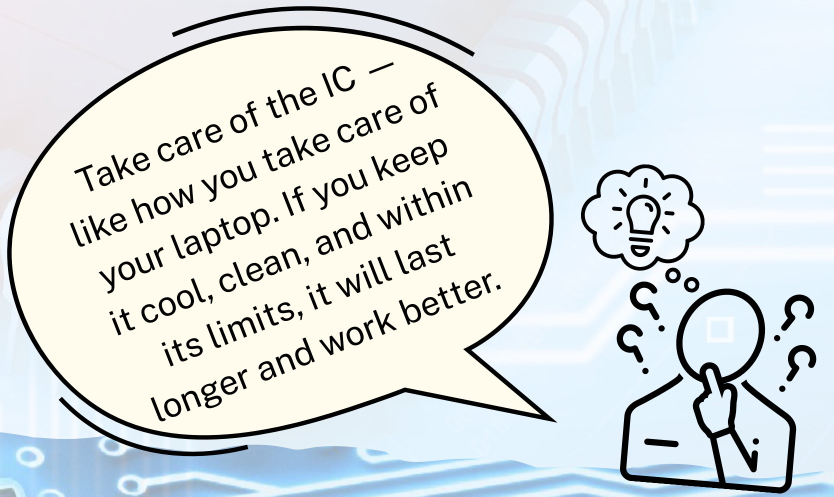
This is the middle and longest phase of the IC's life. During this period, the failure rate is very low and stable. The IC performs its functions reliably if used under proper conditions (temperature, voltage, etc.).

CAUSES FAILURE

- Sudden environmental stress
- Random defects not detected earlier

REDUCE

Use Correct Voltage, Keep it Cool, Avoid Physical Damage, Follow Manufacturer’s Limits, Use Good Quality Parts, Check Performance Regularly



C. Wear out

What is?

This is the final stage of an IC's life, where aging and physical degradation take place. The failure rate increases again as the IC's materials start to wear down due to years of usage.

CAUSES FAILURE

- Electromigration (movement of metal atoms)
- Oxide breakdown
- Thermal stress and fatigue
- Corrosion

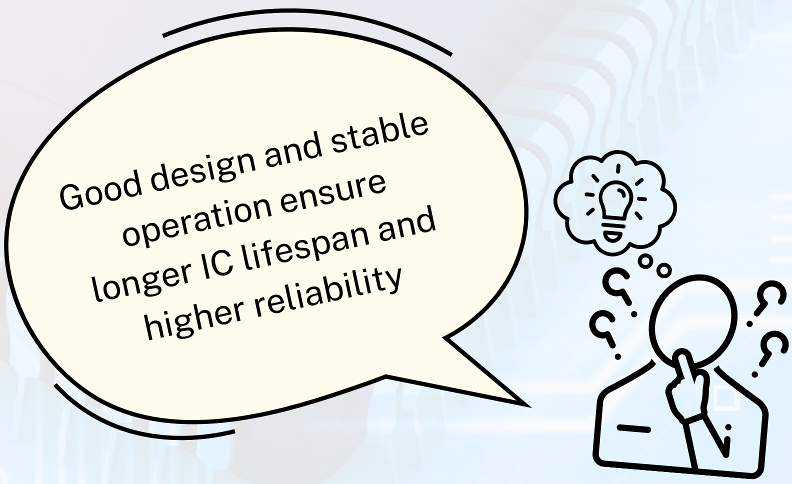
REDUCE

Control the Temperature, Avoid Overuse, Reduce Electrical Stress, Use Quality Materials, Regular Maintenance

To slow down wear-out, keep the IC cool, stress-free, and well-protected — just like taking care of an aging car engine.

Summary

Stage	Failure Rate	Duration	Causes	Prevention Method
Infant Mortality	High	Early life	Manufacturing defects	Burn-in testing
Operating Life	Low	Most of IC life	Random stress/faults	Stable operation
Wear-Out	High	End of lifespan	Aging, material degradation	Replace before failure



DEGRADATION OF IC

IC degradation is an inevitable process, but its effects can be minimized through careful design, testing, and material selection. Understanding how degradation occurs helps engineers predict IC lifespan and ensure long-term device reliability.

4.1 Meaning of Degration

What is?

Degradation refers to the gradual decline in the performance or functionality of an integrated circuit (IC) over time. It happens due to physical, chemical, or electrical stresses that affect the materials and structures inside the chip. Although an IC may pass initial testing, long-term use can slowly reduce its reliability and efficiency.

CAUSES FAILURE

- Temperature Stress
- Electrical Stress
- Environmental Factors
- Material Aging

TYPES

1. **Electromigration**:
   → Movement of metal atoms due to high current density
2. **Time-Dependent Dielectric Breakdown (TDDB)**:
   → Breakdown of insulating oxide over time.
3. **Hot Carrier Injection (HCI)**:
   → High-energy electrons trapped in transistor oxide.
4. **Bias Temperature Instability (BTI)**:
   → Parameter drift due to voltage and temperature stress.

CAUSES FAILURE

- High current density
- Long-term voltage stress
- High-energy carriers in transistor
- Voltage & temperature stress

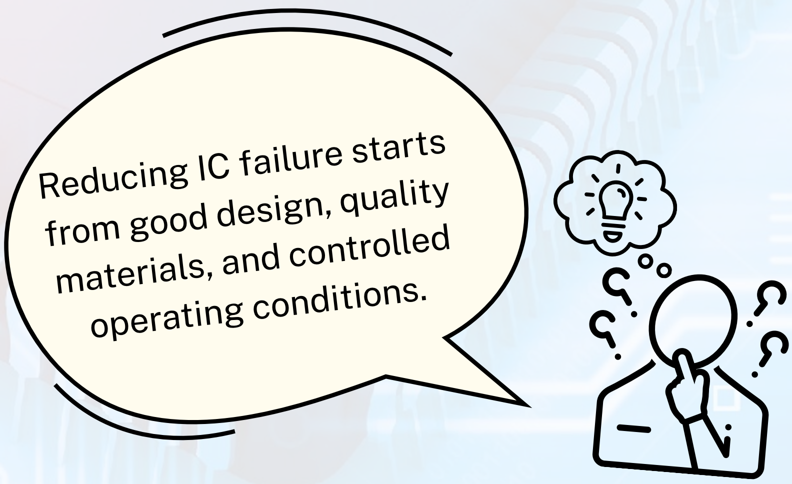
REDUCE

- Use wider metal lines, stronger materials, and limit current flow.
- Use quality oxides and lower operating voltage.
- Reduce supply voltage and improve transistor design.
- Control temperature and use stable materials.

Summary

IC failures can be reduced through better materials, lower voltage, and proper thermal control.

By lowering electrical stress, temperature, and current density, engineers can significantly extend IC lifespan and improve device reliability.



FAILURE ANALYSIS

Sometimes, even after all the testing and quality control, integrated circuits (ICs) can still fail. When this happens, engineers must find out why — this is called failure analysis.

Failure analysis helps improve manufacturing, prevent future issues, and fix product defects.

5.1 General Process Flow in IC Failure Analysis

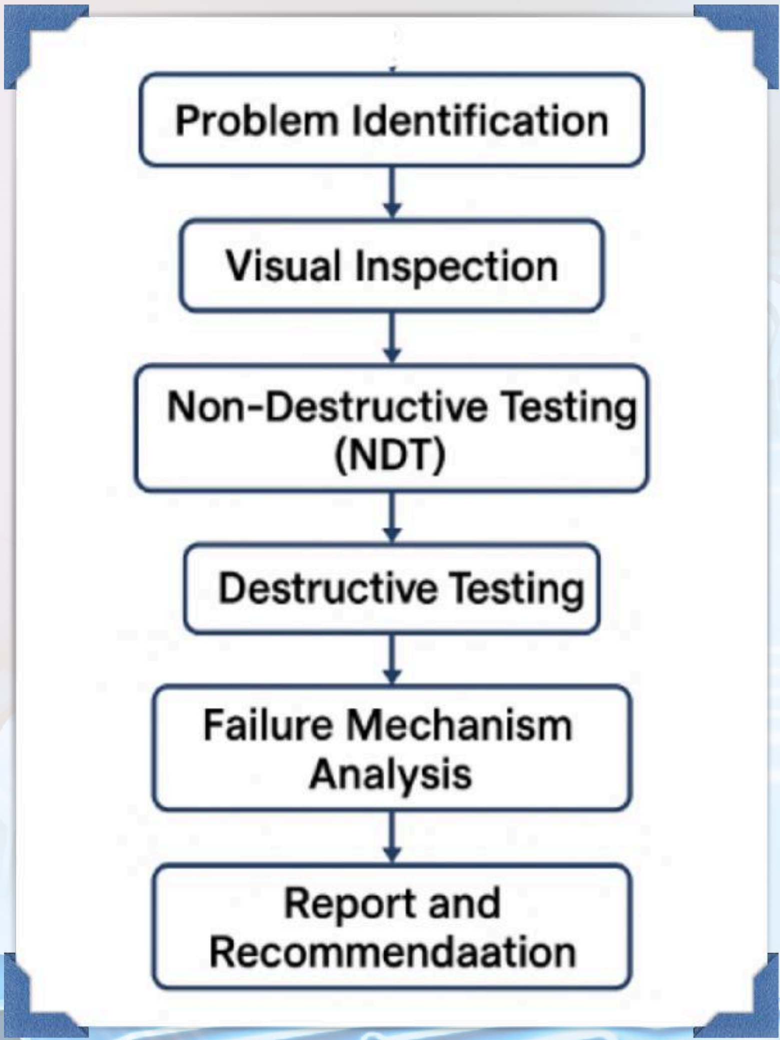


Figure 5.1 : Process Flow in IC Failure Analysis

5.1 General Process Flow in IC Failure Analysis

Failure analysis follows a step-by-step process to find the root cause of the problem. Here's a simplified version of how it works:

- **Problem Identification**
  → Collect information about the failure (e.g. when, how, under what condition it failed).
- **Visual Inspection**
  → Look at the IC under a microscope to check for cracks, burns, broken pins, etc.
- **Electrical Testing**
  → Measure voltage, current, and resistance to locate faults.
- **Non-Destructive Testing (NDT)**
  → Use methods like X-rays to look inside the chip without damaging it.
- **Destructive Testing**
  → If NDT is not enough, physically open the IC to examine internal layers.
- **Failure Mechanism Analysis**
  → Identify how and why the failure happened (e.g., corrosion, metal cracking, overheating).
- **Report and Recommendation**
  → Write a report and suggest how to prevent the same issue in future production.

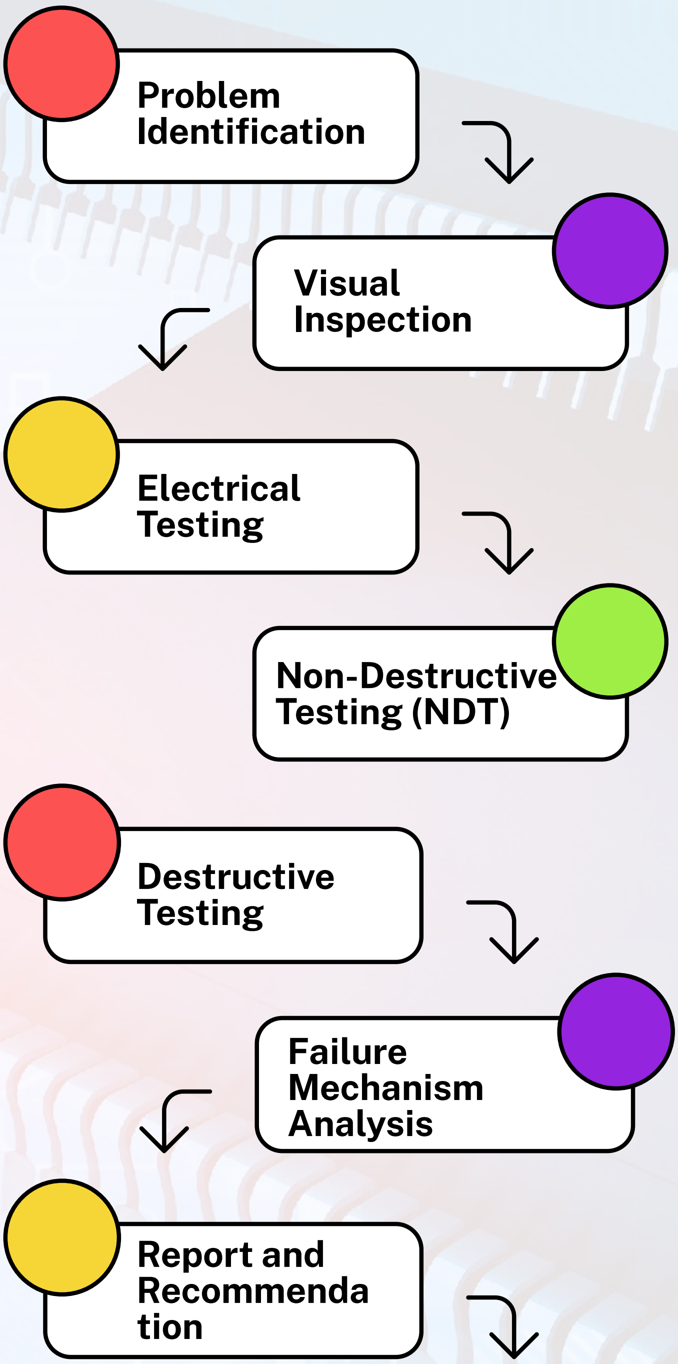


Figure 5.2 : Process Flow in IC Failure Analysis

EXAMPLE

A smartphone IC stops working. Engineers inspect it and find a crack in the bonding wire due to overheating. They recommend better cooling for future versions.

5.2

Test in Failure Analysis

To investigate IC failures, engineers use two types of tests:

1. Non-Destructive Testing (NDT)
2. Destructive Testing

A. Non-Destructive Test (NDT)

What is?

Testing that does not damage the IC. The chip can still be reused after the test.

COMMON METHODS

X-Ray Inspection
→ Checks internal structures and bonding wires.

Infrared Imaging (IR)
→ Detects heat spots caused by internal short circuits.

Acoustic Microscopy
→ Finds cracks, voids, or delamination inside the package.

Scanning Electron Microscope (SEM)
→ High-resolution images of surface details.

B. Destructive Test

What is?

Testing that involves physically damaging or opening the IC to look inside. Once tested, the chip cannot be reused.

COMMON METHODS

Decapsulation
→ Removing the chip's outer casing to inspect the die.

Cross-Sectioning
→ Cutting the chip to view internal layers.

Delayering
→ Removing layers one by one to examine internal circuits.

Chemical Staining
→ Highlights certain defects or structures.

EXAMPLE

- **NDT** = gentle inspection (chip survives)
- **Destructive** = deeper look (chip is sacrificed)

Summary

Test Type	Does It Damage the IC?	Examples	When It's Used
Non-Destructive	No	X-ray, IR, SEM, acoustic	First step in analysis
Destructive	Yes	Decapsulation, slicing	When deeper inspection is

SUMMARY

Integrated Circuits (ICs) go through several stages of testing and analysis to ensure they function correctly and last a long time. In this chapter, we explored the three key areas involved in maintaining the quality and reliability of ICs:

IC TESTING

- ICs are tested at wafer level and after packaging to check for defects.
- Test Pattern Testing uses signal patterns to verify circuit logic.
- Probe Testing contacts each die on the wafer to measure performance.
- Final Testing ensures the packaged IC works correctly before shipping.
- Burn-in Testing stresses ICs under high temperature/voltage to catch early failures.

RELIABILITY

Reliability means the IC performs its job over time without failure.

Engineers use techniques like FMEA to predict possible failure modes and improve design.

The Bathtub Curve explains three failure stages:

- Infant Mortality – early-life defects
- Useful Life – stable, low failure
- Wear-Out – aging-related breakdown

Keeping ICs within safe limits helps reduce wear-out and extend their life.

FAILURE ANALYSIS

- When ICs fail, engineers investigate using Failure Analysis to find the cause.
- The process involves visual checks, electrical tests, NDT, and destructive methods.
- Non-Destructive Tests (NDT) like X-ray and SEM do not damage the chip.
- Destructive Tests like decapsulation and cross-sectioning help uncover hidden internal failures.
- This analysis helps improve future IC design and manufacturing.

Testing, reliability prediction, and failure analysis all work together to make sure ICs are safe, stable, and long-lasting.

VIDEO

IC TESTING
RELIABILITY
FAILURE ANALYSIS

Klik Link below to know more

[Video: Semiconductor Reliability Testing and Why Its Needed]

[Video: Semiconductor Failure Analysis And Why It Is Important]

QUIZ

IC TESTING
RELIABILITY
FAILURE ANALYSIS

Klik Link below to answer this short Quiz

SCAN ME!

Part A

SCAN ME!

Part B

QUIZ

IC TESTING
RELIABILITY
FAILURE ANALYSIS

Klik Link below to answer this short Quiz

(Malay Version)

SCAN ME!

Part A

SCAN ME!

Part B

SCAN ME!

Part C

QUIZ

IC TESTING
RELIABILITY
FAILURE ANALYSIS

Klik Link below to answer this short Quiz

QUIZIZZ

SCAN ME!
Part A

SCAN ME!
Part B

SCAN ME!
Part C

REFERENCES

Taur, Y., Ning, T.H. (2022). **Fundamentals of Modern VLSI Devices**. 3rd Edition. United Kingdom: Cambridge University Press

R. Jacob Baker (2019) **CMOS Circuit Design, Layout and Simulation**, 4th Edition. New Jersey Wiley – IEEE Press. Inc

Shubham, K., Gupta, A. (2021). **Integrated Circuit Fabrication**. London, UK: Taylor & Francis Ltd

Sze, S.M (2021). **Physic Of Semiconductor Devices**. United States: John Wiley and Sons Ltd

Tejinder Gandhi (2019). **Microelectronics Failure Analysis Desk Reference**. 7th Edition. ASM International

Ayers, R. (2019). **Digital integrated circuit design: From VLSI architectures to CMOS fabrication**. CRC Press.

Balakrishnan, V., & Raghavan, S. (2017). **Integrated circuit testing and failure analysis**. Springer.

Gupta, S. K. (2018). **Reliability engineering and life testing.** PHI Learning.

Jaeger, R. C., & Blalock, T. N. (2022). **Microelectronic circuit design** (6th ed.). McGraw-Hill Education.

IEEE Spectrum. (2023). **Understanding IC reliability and testing in modern fabrication**. Retrieved from https://spectrum.ieee.org

Nelson, W., & Meeker, W. Q. (2020). Statistical methods for reliability data (2nd ed.). Wiley.

Semiconductor Engineering. (2023). **Failure analysis and reliability testing techniques**. Retrieved from https://semiengineering.com

Texas Instruments. (2022). **Semiconductor reliability and qualification summary**. Retrieved from https://www.ti.com

IEEE Malaysia Section. (2022). **Advancements in semiconductor reliability testing**. Retrieved from https://ieeemy.org

IC FABRICATION PROCESS

IC TESTING, RELIABILITY & FAILURE ANALYSIS

About This eBook

This eBook introduces readers to the essential concepts of Integrated Circuit Testing, Failure Analysis, and Failure Analysis.

About The Authors

We are a team of educators and innovators dedicated to making semiconductor education accessible and interactive. This eBook was developed as part of a teaching innovation project, aimed at enhancing students' understanding of microelectronics fabrication and reliability testing through engaging digital learning.

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